



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,261	11/03/2003	Jui-Feng Ko	JCLA7806	6081

23900 7590 05/04/2006

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER

SHERMAN, STEPHEN G

ART UNIT PAPER NUMBER

2629

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/701,261

Applicant(s)

KO ET AL.

Examiner

Stephen G. Sherman

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because of improper grammar. The final sentence of the abstract states: "The clock signal is modulated through the algorithm so that electromagnetic interference signal at various frequencies is optimally process." Correction is required. See MPEP § 608.01(b).
2. The disclosure is objected to because of the following informalities: grammar mistakes.

Page 2, line 1 states: "Back in the 1970s, liquid crystal displays **are** used in electronic calculators, clocks and watches."

Page 2, line 3 states: "...improvements in driving techniques **has lead** to the production of..."

Page 2, line 10 states: "Among the panel of tests **a TFT-LCD that needs** to be conducted..."

Page 3, line 1 states: "...includes using the pulse of **an EMI as center** to increase..."

Page 3, lines 5-6 states: "...the EMI signal no longer **pose** a problem..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Sha et al. (US 6,980,581).

Regarding claim 1, Sha et al. disclose a control chip built inside an integrated circuit for reducing electromagnetic interference (Figures 4 and 5), wherein the control chip is able to spread out the frequency of an electromagnetic interference signal according to an algorithm (Figures 5-7 and column 4, lines 37-56 explain that the computer program, or algorithm, allows the circuit 108 to determine the gain adjustment needed to be made according to an output frequency creating an adaptive spread spectrum clock generator that automatically adjusts the PLL behavior when frequency is changed, such that the frequency of an EMI signal can be spread out properly for any frequency as also explained in column 5, lines 50-67.).

Regarding claim 7, Sha et al. disclose a method of reducing the strength of an electromagnetic interference signal, comprising the steps of:

receiving an algorithm (Figures 5 and 7 and column 4, lines 39-56 explain that AGO VCO 108 receives a computer program, or algorithm as shown in Figure 7, and as explained in column 5, lines 30-39 if the computer program is stored then the AGO VCO 108 would have to receive the algorithm from the storage.);

determining a specified frequency of the electromagnetic interference signal and a corresponding spread out width at that frequency according to the algorithm (Figure 5, shows that the feedback divider 116 receives V_{out} from the AGO VCO 108 which then produces the signal FEEDBACK which is input into the spread spectrum circuitry 118 for determining the spread out width at the specified frequency as explained in column 4, lines 13-26.); and

spreading out the electromagnetic interference signal according to the spread out width using the specified frequency as the center of spreading (Column 4, lines 13-26 explain that the ROM codes are optimized for the frequency F_{out} such that the spread spectrum circuitry can properly spread out the width using the frequency F_{out} as the center frequency.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha et al. (US 6,980,581) in view of Yavitz (US 2003/0033385).

Regarding claim 2, Sha et al. disclose the control chip of claim 1.

Sha et al. fail to teach that the control chip picks up the algorithm from an external bus.

Yavitz discloses of a control chip which picks up an algorithm from an external bus (Figure 2 shows that the card 30 picks up application software 76 from an external bus 43 to be applied to the PLL 64 as explained in paragraph [0027]).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made that the computer program used by the control chip taught by Sha et al. would be received from an external bus as taught by Yavitz such that a separate memory for the computer program would not be needed inside the control chip in order to allow for the conservation of space for the control chip such that the control chip can be made smaller.

Regarding claim 3, Sha et al. disclose a control chip for reducing electromagnetic interference, comprising:

a software phase lock loop (Figure 5, item 100. The examiner interprets that since the PLL shown uses an algorithm, as explained in the rejection of claim 1, that it is a SPPL.) built inside the control chip for receiving a clock signal (Figure 5, the phase detector 110 receives REF 102 as explained in column 4, lines 2-3. Column 3, lines 35-46 explain that the output signal Fout is a spread spectrum clock signal with a mean frequency determined by the frequency for the signal REF, and if the signal REF has a frequency then it is a clock signal.) and spreading out the frequency of an electromagnetic interference signal according to an algorithm (Please refer to the explanation used in the rejection of claim 1.).

Sha et al. fail to teach that the control chip comprises a bus coupled to the software phase lock loop for inputting the algorithm.

Yavitz discloses of a control chip which picks up an algorithm from an external bus (Figure 2 shows that the card 30 picks up application software 76 from an external bus 43 to be applied to the PLL 64 as explained in paragraph [0027].).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made that the computer program used by the control chip taught by Sha et al. would be received from an external bus as taught by Yavitz such that a separate memory for the computer program would not be needed inside the control chip in order to allow for the conservation of space for the control chip such that the control chip can be made smaller.

Regarding claim 4, Sha et al. and Yavitz disclose the control chip of claim 3.

Sha et al. also disclose wherein the frequency of the electromagnetic interference signal and the spread out width at that frequency is set by the algorithm within the software phase lock loop (Please refer to the explanation used in the rejection of claim 7.).

Regarding claim 5, Sha et al. disclose an application specific integrated circuit for reducing electromagnetic interference, comprising:

a first input terminal for receiving a clock signal (Figure 5, the phase detector 110 contains an input terminal which receives REF 102 as explained in column 4, lines 2-3. Column 3, lines 35-46 explain that the output signal Fout is a spread spectrum clock

signal with a mean frequency determined by the frequency for the signal REF, and if the signal REF has a frequency then it is a clock signal.); and

a software phase lock loop coupled to the first input terminal (Figure 5 shows the SPLL 100 which receives signal REF as explained above.) for spreading out the frequency of an electromagnetic interference signal according to the clock signal and an algorithm (Please refer to the explanation used in the rejection of claim 1.).

Sha et al. fails to teach of a second input terminal for receiving the algorithm.

Yavitz discloses of a control chip which picks up an algorithm from an external bus of which is input into an input terminal of a PLL (Figure 2 shows that the card 30 picks up application software 76 from an external bus 43 to be applied to the PLL 64 as explained in paragraph [0027].).

Therefore it would have been obvious to “one of ordinary skill” in the art at the time the invention was made that the computer program used by the integrated circuit taught by Sha et al. would be received from an external bus as taught by Yavitz such that the integrated circuit would receive the algorithm at a second input terminal in order to allow for the conservation of space for the control chip such that the control chip can be made smaller while still allowing for the proper functionality of the circuit.

Regarding claim 6, this claim is rejected under the same rationale as claim 4.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

20 April 2006

AMR A. AWAD
PRIMARY EXAMINER

